Form PTO-1449

U.S. Department of Commerce Patent and Trademark Office Attorney's Docket No. 10559-311US1

Application No. 10/070,008

Information Disclosure Statement by Applicant (Use several sheets if necessary) Applicant
Gilbert Wolrich et al.

Filing Date

February 28, 2002

Group Art Unit

(37 CFR §1.98(b))

	U.S. Patent Documents									
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate			
or	AA	09/473,571	12/28/1999	Wolrich et al.						
5	AB	09/475,614	12/30/1999	Wolrich at al.						
	AC									
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	AF									
	AG									

	Foreign Patent Documents or Published Foreign Patent Applications												
Examiner	Desig.	Document	Publication	Country or		_	Translation						
Initial	D	Number	Date	Patent Office	Class	Subclass	Yes	No					
9	AH	WO 01/16697	03/2001	WIPO									
5	ΑI	WO 01/16698	03/2001	WIPO									
2	AJ	WO 01/16702	03/2001	WIPO				_					
2	AK	WO 01/16703	03/2001	WIPO									
6	AL	WO 01/16714	03/2001	WIPO									
0	AM	WO 01/16715	03/2001	WIPO									
67	AN	WO 01/16716	03/2001	WIPO									
2	AO	WO 01/16722	03/2001	WIPO									
2	ΑP	WO 01/16758	03/2001	WIPO									
6	AQ	WO 01/18646	03/2001	WIPO									
	AR												

Other Documents (include Author, Title, Date, and Place of Publication)								
Examiner	Desig.							
Initial	ID	Document						
4	AS	Paver et al., "Register Locking in Asynchronous Processor Computer Design: VLSI Processors," ICCD '92 Proceedings, IEEE 1992 International Conference, 1992, pp. 351-355.						
	- AT	Waldspurger et al., "Register Relocation: Flexible Contents for Multithreading," Proceedings of the 20th Annual International Symposium on Computer Architecture," 1993, pp. 120-130.						
	ΑŪ							

Examiner	Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

1406/04

Title of Invention

BRANCH INSTRUCTION FOR PROCESSOR

Application Number:

10/070008

5753

Confirmation Number: First Named Applicant:

Gilbert Wolrich

Attorney Docket Number:

10559-311US1

Art Unit:

Examiner:

Search string:

(3373408 or 3478322 or 3792441 or 3913074 or 3940745 or 4130890 or 4392758 or 4400770 or 4514807 or 4523272 or 4724521 or 4745544 or 4777587 or 4866664 or 5073864 or 5140685 or 5142683 or 5155831 or 5155854 or 5168555 or 5173897 or 5255239 or 5263169 or 5347648 or 5357617 or 5367678 or 5390329 or 5392391 or 5392411 or 5392412 or 5404464 or 5404482 or 5428809 or 5432918 or 5442756 or 5448702 or 5450351 or 5452437 or 5459842 or 5463625 or 5467452 or 5481683 or 5487159 or 5517628 or 5517648 or 5542070 or 5542088 or 5544236 or 5550816 or 5557766 or 20020053017 or 20020056037 or 20030041228 or 20030145159 or 20030191866 or 20040039895 or 20040054880 or 20040071152 or 20040073728

or 20040073778 or 20040098496 or 20040109369 or 20040205747).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
ん	1	3373408	1968-03-12	Ling	-		
4	2	3478322	1969-11-11	Evans			
ん	3	3792441	1974-02-12	Wymore et al.			
٦,	4	3913074	1975-10-14	Homberg et al.			
1	5	3940745	1976-02-24	Sajeva			
2	6	4130890	1978-12-19	Adam			
れ	7	4392758	1983-07-12	Bowles et al.			
ヘ	8	4400770	1983-08-23	Chan et al.			
2	9	4514807	1985-04-30	Nogi			-
2	10	4523272	1985-06-11	Fukunaga et al.			
7	11	4724521	1988-02-09	Carron et al.			
1	12	4745544	1988-05-17	Renner et al.			
4	13	4777587	1988-10-11	Case et al.			
7	14	4866664	1989-09-12	Burkhardt Jr. et			
		<u> </u>		al.			
ሗ	15	5073864	1991-12-17	Methvin et al.			
	16	5140685	1992-08-18	✓ Sipple et al.			

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	17	5142683	1992-08-25	Burkhardt Jr. et	_		
12				al.			
8	18	5155831	1992-10-13	Emma et al.			
n	19	5155854	1992-10-13	Flynn et al.			
w	20	5168555	1992-12-01	Byers et al.			
1	21	5173897	1992-12-22	Schrodi et al.			
a	22	5255239	1993-10-19	Taborn et al.			
9	23	5263169	1993-11-16	Genusov et al.			
a	24	5347648	1994-09-13	Stamm et al.			
U	25	5357617	1994-10-18	Davis et al.			
1/1	26	5367678	1994-11-22	Lee et al.			
2	27	5390329	1995-02-14	Gaertner et al.			
n	28	5392391	1995-02-21	Caulk Jr. et al.			
N	29	5392411	1995-02-21	Ozaki			
1	30	5392412	1995-02-21	McKenna			
9	31	5404464	1995-04-04	Bennett			
01	32	5404482	1995-04-04	Stamm et al.			
1	33	5428809	1995-06-27	Coffin et al.			
2	34	5432918	1995-07-11	Stamm			
2	35	5442756	1995-08-15	Grochowski et al.			
7	36	5448702	1995-09-05	Garcia Jr. et al.			
n	37	5450351	1995-09-12	Heddes			
2	38	5452437	1995-09-19	Richey et al.			
6	39	5459842	1995-10-17	Begun et al.			
9/	40	5463625	1995-10-31	Yasrebi			
a	41	5467452	1995-11-14	Blum et al.			
9	42	5481683	1996-01-02	Karim			
1	43	5487159	1996-01-23	Byers et al.			
a	44	5517628	1996-05-14	Morrison et al.	 		
2	45	5517648	1996-05-14	Bertone et al.			
2	46	5542070	1996-07-30	LeBlanc et al.	 		
1/2	47	5542088	1996-07-30	Jennings Jr. et			
V				al.		<u> </u>	
a	48	5544236	1996-08-06	Andruska et al.			
1	49	5550816	1996-08-27	Hardwick et al.			
2	50	5557766	1996-09-17	Takiguchi et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
1/1	1	20020053017	2002-05-02	Adiletta et al.	_		
6	2	20020056037	2002-05-09	Wolrich et al.			
13	3	20030041228	2003-02-27	Rosenbluth et al.			
4	4	20030145159	2003-07-31	Adiletta et al.			
2	5	20030191866	2003-10-09	Wolrich et al.			

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in	6	20040039895	2004-02-26	Wolrich et al.	Γ.	
7	7	20040054880	2004-03-18	Bernstein et al.		
2	8	20040071152	2004-04-15	Wolrich et al.		
2	9	20040073728	2004-04-15	Wolrich et al.		
5	10	20040073778	2004-04-15	Adiletta et al.		
3	11	20040098496	2004-05-20	Wolrich et al.		
4	12	20040109369	2004-06-10	Wolrich et al.		
	13	20040205747	2004-10-14	Bernstein et al.		

Signature

Examine Name Date

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

2/36/24

Title of Invention

BRANCH INSTRUCTION FOR PROCESSOR

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5753

First Named Applicant:

Gilbert Wolrich

Attorney Docket Number:

10559-311US1

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Search string:

(5568617 or 5574922 or 5574939 or 5592622 or 5606676 or 5613071 or 5613136 or 5623489 or 5627829 or 5630130 or 5644623 or 5649157 or 5659722 or 5680641 or 5689566 or 5692167 or 5699537 or 5717898 or 5721870 or 5742587 or 5742782 or 5742822 or 5745913 or 5751987 or 5761507 or 5761522 or 5781774 or 5784649 or 5784712 or 5796413 or 5797043 or 5809235 or 5809530 or 5812839 or 5812868 or 5828746 or 5828863 or 5832215 or 5835755 or 5854922 or 5860158 or 5886992 or 5887134 or 5890208 or 5892979 or 5905876 or 5905889 or 5915123 or 5933627

or 5659687).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
4	1	5568617	1996-10-22	Kametani			,
	2	5574922	1996-11-12	James			
4	3	5574939	1996-11-12	Keckler et al.			
5	4	5592622	1997-01-07	Isfeld et al.			
4	5	5606676	1997-02-25	Grochowski et al.			
2	6	5613071	1997-03-18	Rankin et al.			
6	7	5613136	1997-03-18	Casavant et al.			
4	8	5623489	1997-04-22	Cotton et al.			
4	9	5627829	1997-05-06	Gleeson et al.			
6	10	5630130	1997-05-13	Perotto et al.			
1	11	5644623	1997-07-01	Gulledge			i
2	12	5649157	1997-07-15	Williams			
6	13	5659722	1997-08-19	Blaner et al.			
4	14	5680641	1997-10-21	Sidman			
6	15	5689566	1997-11-18	Nguyen			
	⁄ 16	5692167	1997-11-25	Grochowski et al.			
$\lceil 7 \rceil$	17	5699537	1997-12-16	Sharangpani et			
$ \mathcal{L} $	//	7 /	7	al.			

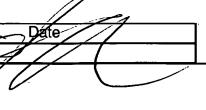
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					. 1 1
4	18	5717898	1998-02-10	Kagan et al.	
N	19	5721870	1998-02-24	Matsumoto	
V	20	5742587	1998-04-21	Zornig et al.	
1	21	5742782	1998-04-21	Ito et al.	
42	22	5742822	1998-04-21	Motomura	
n	23	5745913	1998-04-28	Pattin et al.	
1	24	5751987	1998-04-12	Mahant Shetti et	
				al.	
M	25	5761507	1998-06-02	Govett	
6	26	5761522	1998-06-02	Hisanaga et al.	 _
n	27	5781774	1998-07-14	Krick	
W	28	5784649	1998-07-21	Begur et al.	
0	29	5784712	1998-07-21	Byers et al.	
1	30	5796413	1998-08-18	Shipp et al.	
6	31	5797043	1998-08-18	Lewis et al.	
1	32	5809235	1998-09-15	Sharma et al.	
3	33	5809530	1998-09-15	Samra et al.	
27	34	5812839	1998-09-22	Hoyt et al.	
a	35	5812868	1998-09-22	Moyer et al.	
6	36	5828746	1998-10-27	Ardon	
5/	37	5828863	1998-10-27	Barrett et al.	
	38	5832215	1998-11-03	Kato et al.	
1	39	5835755	1998-11-10	Stellwagen Jr.	
2	40	5854922	1998-12-29	Gravenstein et	
		·		al.	
N	41	5860158	1999-01-12	Pai et al.	
12	42	5886992	1999-03-23	Raatikainen et	ŀ
	- 40	5007404	1000 00 00	al.	
5	43	5887134	1999-03-23	Ebrahim	
5	44	5890208	1999-03-30	Kwon	
~	45	5892979	1999-04-06	Shiraki et al.	
2	46	5905876	1999-05-18	Pawlowski et al.	
5	47	5905889	1999-05-18	Wilhelm Jr.	
	48	5915123	1999-06-22	Mirsky et al.	
6	49	5933627	1999-08-03	Parady	
0	50	5659687	1997-08-19	Kim et al.	

Signature

Examiner Name



ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Stylesheet Version v18.0

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or 5450603).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

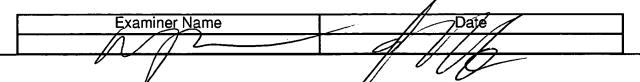
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
5	1	6223238	2001-04-24	Meyer et al.			•
4	2	6223279	2001-04-24	Nishimura et al.			
2	3	6247025	2001-06-12	Bacon			
2	4	6256713	2001-07-03	Audityan et al.			
4	5	6272616	2001-08-07	Fernando et al.			
1	6	6275505	2001-08-14	O Loughlin et al.			
8	7	6279113	2001-08-21	Vaidya			
W	8	6289011	2001-09-11	Seo et al.			
9	9	6298370	2001-10-02	Tang et al.			
2	10	6307789	2001-10-23	Wolrich et al.			
2	11	6324624	2001-11-27	Wolrich et al.			
2	12	6345334	2002-02-05	Nakagawa et al.			
1	13	6347344	2002-02-12	Baker et al.		_	
9	14	6351808	2002-02-26	Joy et al.			
2	15	6356962	2002-03-12	Kasper et al.			
6	16	6373848	2002-04-16	Allison et al.			
9	17	6360262	2002-03-19	Guenthner et al.	,		
4	18	6389449	2002-05-14	Nemirovsky et al.	1		

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N	19	6393483	2002-05-21	Latif et al.		
1/2	20	6415338	2002-07-02	Habot		
1/1	21	6426940	2002-07-30	Seo et al.		
6	22	6427196	2002-07-30	Adiletta et al.		
1	23	6430626	2002-08-06	Witkowski et al.		Ĭ i
2	24	6434145	2002-08-13	Opsasnick et al.		
9	25	6463072	2002-10-08	Wolrich et al.		
2	26	6532509	2003-03-11	Wolrich et al.		
4	27	6552826	2003-04-22	Adler et al.		
a	28	6560667	2003-05-06	Wolrich et al.		
an	29	6577542	2003-06-10	Wolrich et al.		
92	30	6584522	2003-06-24	Wolrich et al.		
2	31	6587906	2003-07-01	Wolrich et al.		
9	32	6606704	2003-08-12	Adiletta et al.		
2	33	6625654	2003-09-23	Wolrich et al.		
n	34	6629237	2003-09-30	Wolrich et al.		
2	35	6631430	2003-10-07	Wolrich et al.		Î
2	36	6631462	2003-10-07	Wolrich et al.		
14	37	6661794	2003-12-09	Wolrich et al.		
	38	6667920	2003-12-23	Wolrich et al.		
7	39	6668317	2003-12-23	Bernstein et al.		
n	40	6681300	2004-01-20	Wolrich et al.		
a	41	6694380	2004-02-17	Wolrich et al.		
W	42	4023023	1977-05-10	Bourrez et al.		
	43	5113516	1992-05-12	Johnson		
(1)	44	5363448	1994-11-08	Koopman Jr. et		
00				al.		
1	45	5436626	1995-07-25	Fijiwara		
2	46	5600812	1997-02-04	Park		
2	47	5652583	1997-07-29	Kang		
4	48	5717760	1998-02-10	Satterfield	ļ .	
4	49	4992934	1991-02-12	Portanova et al.		
4	50	5450603	1995-09-12	Davies		

Signature



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U.S. Department of Commerce Patent and Trademark Office Attorney's Docket No. 10559-311US1

Application No. 10/070,008

Sheet <u>1</u> of <u>2</u>

Information Disclosure Statement

by Applicant (Use several sheets if necessary) Applicant Gilbert Wolrich et al.

Filing Date February 28, 2002 **Group Art Unit**

(37 CFR §1.98(b))

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner	Desig.	Document	Publication	Country or			Translation	
Initial	ID	Number	Date	Patent Office	Class	Subclass	Yes	No .
in	AA	WO 01/50679	07/12/2001	WIPO				·
4	AB	WO 01/50247	07/12/2001	WIPO				
2	AC	WO 01/48619	07/05/2001	WIPO				
h	AD	WO 01/48606	07/05/2001	WIPO		· ·		
2	AE	WO 01/48599	07/05/2001	WIPO				
W	AF	WO 01/48596	07/05/2001	WIPO				
V	AG	WO 01/41530	06/14/2001	WIPO				
2	AH	WO 01/16782	03/08/2001	WIPO				
9	AI	WO 01/16770	03/08/2001	WIPO				
a	AJ	WO 01/16769	03/08/2001	WIPO				
2	AK	WO 01/16718	03/08/2001	WIPO				
6	AL	WO 01/15718	03/08/2001	WIPO				
6	AM	WO 97/38372	10/16/1997	WIPO				
12	AN	WO 94/15287	07/07/1994	WIPO				
2	AO	EP 0 809 180	11/26/1997	Europe				
_	AP	EP 0 745 933	12/04/1996	Europe				
h	AQ	EP 0 633 678	01/11/1995	Europe				
	AR	EP 0 464 715	01/08/1992	Europe				
4	AS	EP 0 379 709	08/01/1990	Europe				
~	AT	59111533	06/27/1984	Japan				

Other Documents (include Author, Title, Date, and Place of Publication)						
Examiner	Desig.	·				
Initial	ID	Document				
0	AU	Agarneal et al., "April: A Processor Architecture for Multiprocessing," Proceedings of the 17 th Annual International Symposium on Computer Architecture, IEEE, pp. 104-114.				
6	AV	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.				
	AW	Chang et al., "A New Mechanism For Improving Branch Predictor Performance," IEEE, pp. 22-31 (1994).				

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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 $O \times Sheet 2 of 2$

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(37 CFR §1.98(b))

February 28, 2002

Examiner Design		Other D	ocuments (include Author, Title, Date, and Place of Publication)
Doyle et al., Microsoft Press Computer Dictionary, 2 nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326. AY Farka et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159. AZ Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156. Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ABB Hauge et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ACC Hauger et al., "Carp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AFE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3.Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architecture," International Journal of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. Trimberger et al, "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 5 th Annual Hawaii International Conference on System Sciences, 199			D
AX USA, 1994, p. 326. AY Farkas et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159. AZ Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156. Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ABB Hause et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. AFF Intel, "11-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keekler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHL Litch et al., "StongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 154-1. ALL Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Timberger et al., "A Th	initial	טו	
AZ Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156. Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ABB Hauser et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ACC Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hannessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. AFF 11, "14.64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. Mendelson et al., "Design Alternatives of Multithreaded Architecture." International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. Trimberger et al., "A time-multiplexed PFQA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. Vibhatavanijt et al., "Simultaneous	or	AX	USA, 1994, p. 326.
AAA Test of the TRAP Protocol," Journal of Parallel and Distributed Computing: Design and Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ABB Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ACC Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. AJJ Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online!, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Trimberger et al., "A Time-Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanij et al., "S	4	AY	
AAA Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ABB Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ACC Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hannessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. AFF J., 1-16 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Trimberger et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. ANN Turner et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. Trimberger et al., "A Time multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et		AZ.	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
ABB FPGAs for Custom Computing Machines, 1998. ACC Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual 1EEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. AFF Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online1, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Turner et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	4	AAA	Test of the TRAP Protocol," Journal of Parallel and Distributed Computing, Academic Press,
Annual 1EEE Symposium on Field-Programmable Custom Computing Machines, 1997. ADD Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482. AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3,Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Onlinel, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.	2	ABB	
AEE Hyde, R., "Overview of Memory Management," Byte, vol. 13, no. 4, 1998, pp. 219-225. AFF Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Onlinel, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. Wallow, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wallowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	N	ACC	
AFF Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21. AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online!, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. ALL Termblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. Waller, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.	12	ADD	
AGG Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Onlinel, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Timberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.	2	AEE	
AGG IEEE, June 1998. AHH Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3,Plenum Press, New York, USA, June 1999, pp. 161-193. AJJ Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online!, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.	V	AFF	31, 7-116 to 7-118 and c-21.
AII Mendelson et al., "Design Alternatives of Multithreaded Architecture," International Journal of Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. AJJ Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Onlinel, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.	0	AGG	
All Parallel Programming, vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193. AJJ Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online!, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. ACO Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	1	АНН	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
Communication Subsystems," Internet Document, Online!, 13 November 1998. AKK Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. ALL Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	6	AII	
ALL Itemolay et al., A Three Dimensional Register File for Superscalar Processors, IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	2	AJJ	
ALL Itemolay et al., A Three Dimensional Register File for Superscalar Processors, IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. AMM Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998. ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	6	AKK	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
ANN Turner et al., "Design of a High Performance Active Router," Internet Document, Online, 18 March 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. APP Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	12	ALL	of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
ANN 1999. Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7. Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs	Co	AMM	Field-Programmable Custom Computing Machines," 1998.
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	W	APP	1989), pp. 1-7.
/ Account Company Community (1978)		AQQ	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

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Date Considered

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Application No.

Information Disclosure Statement by Applicant (Use several sheets if necessary)

Applicant

Gilbert Wolrich et al.

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February 28, 2002

U.S. Patent Documents							
Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	5,812,839	09/22/1998	Hoyt et al.			
	AB	6,009,515	12/28/1999	Steele, Jr.			
	AC	6,076,158	06/13/2000	Sites et al.			
	AD	6,079,014	06/20/2000	Papworth et al.			
	AE	6,115,811	09/05/2000	Steele, Jr.			
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Foreign Patent Documents or Published Foreign Patent Applications								
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Other Documents (include Author, Title, Date, and Place of Publication)					
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	AQ	Chang et al., "Branch Classification: a New Mechanism fro Improving Branch Predictor Performance", ACM 1994, pgs 22 - 31			
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